an image of the mask on a wafer. In this case, the writing accuracy of the mask writing tool may be a main cause of the dimension error.--

Please replace the following paragraph beginning on page 11, line 20, with the following text:

--Moreover, subjecting a peripheral portion of a selected unexposed portion to multiple shot exposure can enhance the accuracy of the dimension of the unexposed portion without significantly reducing the throughput. In addition, the present invention enables exposure of a particular portion with no butting portions, thereby enabling forming of a pattern with little edge roughness and remarkable accuracy of dimension.--

IN THE CLAIMS

Please cancel claims 1-13 without prejudice.

Please amend the claims as follows:

15. (Amended) The apparatus according to claim 14, wherein the positioning means causes the second area in which the butting portions of the unit regions are formed, to correspond to an isolation region employed in the semiconductor device.

16. (Amended) The apparatus according to claim 14, wherein the positioning means determines the position of the beam such that the second area in which the predetermined characteristics of the predetermined function are determined by the pattern width of the exposed region corresponds to an active region incorporated in a transistor in the semiconductor device.

17. (Amended) The apparatus according to claim 14, wherein the positioning means determines the position of the beam such that the region in which the predetermined